COMPARATIVE EVALUATION OF MCM AND WSI SCHEMES FOR IMPLEMENTING A MODULARLY CONFIGURED ATTACHED PROCESSOR ARCHITECTURE

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ABSTRACT

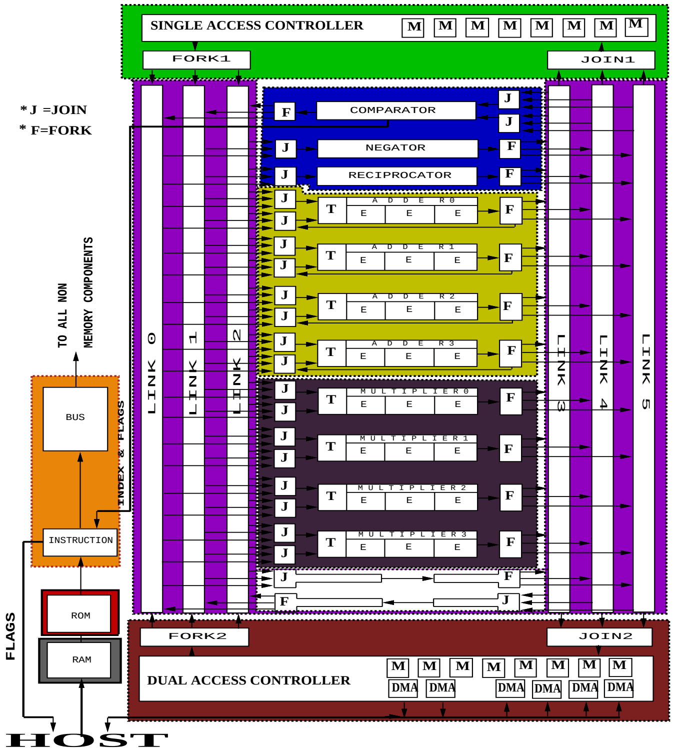
High speed computers often employ attached processors for obtaining enhanced performance. In such a system,"the host is a program manager which handles all I/O, code compiling, and operating system functions, while the attached processor concentrates on arithmetic computation with data supplied by the host." [1] In addition to fast speed, it is also desirable to execute as broad a set of algorithms as possible in order to create a more generally applicable processor. Thus, the underlying goal of the designer is to efficiently utilize the hardware for as broad a set of algorithms as possible. This constraint usually leads to a reduced utilization for most algorithms. Thus, for most current designs, the average sustainable execution rates have been found to be only 5% to 20% of their peak rates, which are determined by summing the maximum computational rates of the processing elements. For example, the sustainable rates for the Cray X-MP with four processors may be as low as 5% for some algorithms [2].

In this paper we present designs for implementing a class of high performance modularly configured attached processors called MCAPs [3] [4] [5], which can attain high speed and high utilization through: (1) closely matching their architectures to the set of algorithms they are to execute,(2) overlapping of processing and memory accessing by using memory prefetching,(3) minimizing the movement of data,(4) using a high-speed CMOS, and(5) having the whole MCAP on a single MCM or wafer.

We start with the transistor count, chip level design using the modified SUSPENS model, then the output driver design and, finally, evaluate various design options for implementing this MCAP architecture using CMOS logic for various Multichip Modules (MCM-L, MCM-C, MCM-D) and Wafer Scale Integration (WSI). This is followed by a quantitative comparision of the various aspects of this MCAP for the MCM and WSI schemes. Matrix multiplication is also evaluated using this MCAP for various packaging schemes.

In all the implementation of a modularly configured attached processor (MCAP) architecture on Multichip Module (MCM-L, MCM-C, MCM-D) and Wafer Scale Integration (WSI) schemes was comparatively evaluated. Delay, area, and power calculations were done for 1 μm, 0.5 μm, and 0.25 μm CMOS technologies. Delay calculations showed that MCAP modules, on average, would achieve a peak performance of 1 GFLOPS. The single-access memory controller component chip (S-control) was found to be the slowest, 110 MHz for 1 μ, 160 MHz for 0.5 μ, and 220 MHz

for 0.25 μ CMOS. The areas were optimized for power densities, low enough to allow air cooling. The example MCAP architecture is shown below.



An Example MCAP Architecture.

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